ABSTRACT

A data processor of the present invention efficiently performs decision processing on register conflict. The data processor contains n-bit instructions and 2n-bit instructions in an instruction set and includes an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the instructions. The 2n-bit instructions including register specification fields have the register specification fields in the first half n bits thereof, and the register specification fields in the first half n bits comprise the same placement as register specification fields in the n-bit instructions. Shift operations required to cut out the register specification fields from the instructions, either 2n-bit or n-bit instructions, can be simplified or deleted by aligning the register specification fields in the 2n-bit instructions with those in the n-bit instructions.